



Attorney Docket No. 1687.1004

*cefc*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Koichiro ISHIBASHI et al.

Application No.: 10/618,710

Confirmation No.: 4927

Filed: July 15, 2003

U.S. Patent No.: 6,864,539 *B2*

Issued: March 8, 2005

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE HAVING BODY BIASING  
CIRCUIT FOR GENERATING FORWARD WELL BIAS VOLTAGE OF SUITABLE  
LEVEL BY USING SIMPLE CIRCUITRY

ATTENTION

CERTIFICATE OF CORRECTION

BRANCH

Batch No.:

Certificate

SEP 06 2005

of Correction

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents  
PO Box 1450  
Alexandria, VA 22313-1450

Sir:

Certificate

SEP 06 2005

of Correction

Patentee(s) respectfully request(s) that a Certificate of Correction be issued in the  
subject patent, pursuant to 35 U.S.C. §254 and 37 C.F.R. §1.322, to correct the mistake(s)  
shown on the attached Form PTO-1050.

Since the mistakes are Patent Office mistakes, it is believed that no fee is required.

Respectfully submitted,

STAAS & HALSEY LLP

Date:

*Aug 31, 2005*

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SEP 07 2005

UNITED STATES PATENT AND TRADEMARK OFFICE  
CERTIFICATE OF CORRECTION

PATENT NO : 6,864,539 *B2*

DATED : March 8, 2005

INVENTOR(S) : Koichiro ISHIBASHI et al.

Title Page,

Inventors:  
change "Koichiro Ishibashi, Warabi (JP)" to --Koichiro Ishibashi, Warabi-shi (JP)--;

OTHER PUBLICATIONS

change "S. Narendra et al., "1.1V 1GHz Communications Router with On-Chip Body Bias 150nm CMOS," ISSCC 2002/ Session 16/High Speed I/O 16.4, pp. 270, 271,466, Feb. 2002." to

-- S. Narendra et al., "1.1V 1GHz Communications Router with On-Chip Body Bias 150nm CMOS," ISSCC 2002/ SESSION 16/HIGH SPEED I/O 16.4, pp. 270, 271,466, Feb. 2002 --.

Column 19,

line 36, (claim 22, line 5) after "MISFET" insert --,--.

Column 20,

line 21, (claim 23, line 31) change "cower" to --power--.

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PATENT NO. 6,864,539

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